REMARKS

Claims 1-10, 12-23, 25, 26, and 51-79 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 112

Claims 1-10, 12-23, 14-23 and 25-26 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. This rejection is respectfully traversed.

The Examiner alleges that the recitation of "a register file" is not enabled because a register file "is a data/software file" and Applicants' claims recite the register file as a hardware element. Applicants respectfully note that the term "register file" can be used to describe a device that includes hardware elements.

Applicants' specification defines the register file as including hardware elements. For example, "[g]eneral purpose registers or a "register file" are a useful component of a data processing system's processing architecture." (See Paragraph [002]). Further, "a general purpose register or "register file" scheme inefficiently accesses registers by requiring access to separate memory units for different processor modes." (See Paragraph [0004]). Applicants use the term "register file" to refer to a register filing scheme throughout the specification. Applicants respectfully note that the claims should be examined using Applicants' intended meaning as stated in the specification. MPEP § 2173.05(a).

As such, Applicants respectfully submit that the claims are enabled.

REJECTION UNDER 35 U.S.C. § 102

Claims 1-10, 14-23, 57-58 and 60-79 are rejected under 35 U.S.C. § 102(b) as being anticipated by Jaggar (U.S. Pat. No. 5,701,493). This rejection is respectfully traversed.

With respect to claim 1, Jaggar fails to show, teach, or suggest a plurality of address encoders, a respective one of the plurality of address encoders for each of the input ports, each of the address encoders to provide an encoded address for accessing one of the memory locations. Instead, Jaggar appears to disclose input ports that share a single alleged address encoder.

For anticipation to be present under 35 U.S.C §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. Scripps *Clinic &* Res. *Found. V. Genentech, Inc., 18* USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be inherent or expressly disclosed and must be arranged as in the claim. *Constant v. Advanced Micro-Devices. Inc.,* 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, Jaggar fails to disclose the limitation of **a plurality of address encoders**, a respective one of the plurality of address encoders for each of the input ports.

As shown in an exemplary embodiment in FIG. 4 of the present application, a register file 206 includes a register file memory unit 400 and a plurality of address encoders including, for example, address encoders 402_1, 402_2, 4023, 402_4, 4101, and 410_2. Each of the address encoders receives a plurality of inputs. For example, the address encoder 402, receives a processor mode input and a srcl.index input. In other

words, each of the inputs to the register file memory unit 400 includes a corresponding address encoder.

As best understood by Applicants, Jaggar does not disclose this limitation. For example, with respect to claim 11, the Examiner alleges that Jaggar discloses "an address encoder to provider an encoded address" (emphasis added), relying on "the combination of components 12-20 in Fig. 8." Applicants respectfully note that FIG. 8 of Jaggar does not disclose **a plurality of address encoders** as claim 1 recites. Instead, as best understood by Applicants, FIG. 8 of Jaggar discloses a single alleged address encoder (i.e. the components 12-20) for all of the registers.

For example, the Examiner indicates an interpretation that the same alleged address encoder corresponds to each of the input ports. (See Page 5, Lines 1-2 of the Office Action). Applicants respectfully submit that this interpreted structure is not analogous to **a plurality of address encoders, a respective one of the plurality of address encoders for each of the input ports**.

Applicants would like to respectfully note that claims 51, 64, 74, and 78 previously included the limitation "a plurality of address encoders." In other words, these claims included this limitation prior to the present rejection, and, as such, the rejection of these claims in the present action is improper.

Applicants respectfully submit that claim 1, as well as its dependent claims, should be allowable for at least the above reasons. Claims 14, 51, 64, 74, and 78, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

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